STUDER D820X
TLS-4000 MKII

INTERFACE DOCUMENTATION

Interface number : 1.812.436.23
IF - Doc number : 10.27.0952

Prepared and edited by
STUDER INTERNATIONAL
(a division of STUDER REVOX AG)
TECHNICAL DOCUMENTATION
Althardstrasse 10
CH-8105 Regensdorf-Zürich

Order No: 10.27.0952 (Ed. 0292)

Summary

1 General Information

1.1 Ordering Information

Order number

- Interface Set
  (Including Interface, Cable and Documentation) 21.812.436.23
- Interface Board (Hardware/Software) 1.812.436.23
- Software Set 1.812.969.23
- IF Cable Studer MKII 1.5m or 1.023.752.00
  IF Cable Studer MKII 5m 1.023.758.00

1.2 Slave Model

- STUDER D820X Digital Audio Tape Recorder

1.3 Software

- First release (Index 20) 1.812.969.20 (04/89)
- Update Index 21 1.812.969.21 (21/89)
- Update Index 22 1.812.969.22 (32/89)
- Update Index 23 1.812.969.21 (03/92)
  SW improvements concerning reliability

2 Installing Procedures

2.1 TLS 4000 Requirements

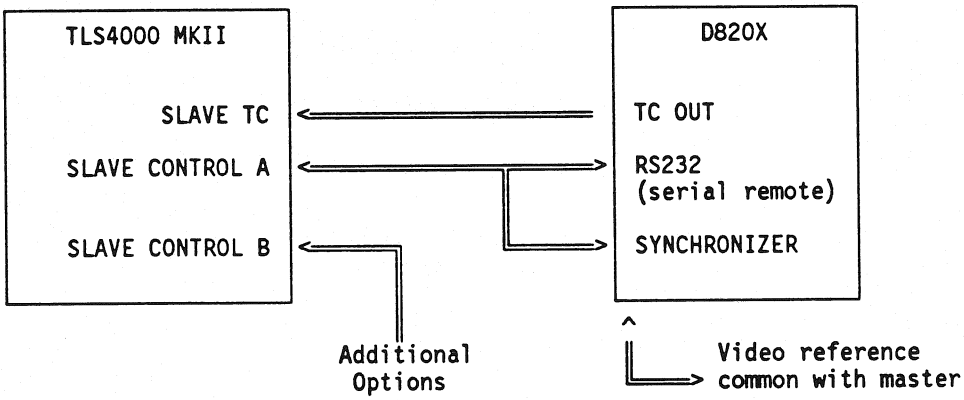
Order number

- Synchronizer Board — 1.812.320.23 or later
- Interface: — correct setup of the DIL switches (see 3.3)

2.2 Slave Requirements

- including Serial Remote Control (RS232), "no echo mode" (menue setting)
- Synchronizer Mode "ON" (is preset by TLS)
- "External Sync" configuration (e.g. video)
- D820X SW release: master 18.1.89
  syscon 23.1.89
- for startup procedure see section 3.6

2.3 Connection Slave-Synchronizer



2.4 Quick Test, Adjustments

Insert the Interface after switching off the synchronizer. Connect the slave machine and switch on synchronizer and slave.

During the first 5 seconds the interface will perform a short selftest. The result is commented with some led messages. If no errors have been found, the display is available for operation messages (see section 3.5)

A correctly recorded timecode on tape is essential for synchronizer operation and should be checked for master and slave (e.g. difference is constant when master ans slave are in PLAY mode).

No adjustments are necessary.

3 Operating Instructions

3.1 Technical Specifications

- Slave type:
  - Digital Audio Tape Recorder
  - SMPTE/EBU timecode (during PLAY) and movepulse information.
  - GOTO with PLAY-STOP sequence
  - Chase-Stop with direct parking
  - transition Chase to Playsync direct
- Tapedeck control:
  - with serial communication
  - movepulse information: direction (LOW = forward) and clock (512Hz @ fs = 48kHz)
- Capstan control:
  - 10.017kHz @ fs = 48kHz

Compensation of Record Dropin/out Delays:
- 224/240msec dropin/dropout @ 48kHz
- 235/243msec dropin/dropout @ 44.1kHz

Compensation of distance between audio and timecode head:
- 119msec @ 48kHz
- 130msec @ 44.1kHz

- Sync accuracy: < 200usec
- Park accuracy: 20msec
- Lock time: (in CUED status, Master Start - SYNC): typ. 3 sec

3.2 Summary of Supported Functions

Tape Deck Commands:

- STOP
- PLAY — nominal
  external varispeed (0.7...1.25 vnom)
  internal varispeed (±12.5%)
- REC
- EDIT — same as STOP
- FORW, REW — with variable speed (0...vmax)
- SHTLF, SHTLR — same as FORW/REW, but with LIFTER defeated
- LOC, LOCREL — performed with the D820X locator
- REHEARSE, MUTE, KEYBOARD:
  available
- EVENT Relay: available (see section 3.4)
- CONDITIONAL COMMANDS:
  available with tape deck commands (STOP...SHTLR), rehearse, mute and relay commands.
- STATUS Request:
  Status information is updated periodically by means of parallel communication.
- AUDIO Channel Control:
  Is available for READY/SAFE selection with the following track assignment:

  CHANNEL 1 = Audio Track 1
  CHANNEL 2 = Audio Track 2
  CHANNEL 3 = TC Track
- TRANSPARENT Commands:
  ASCII command strings can be sent directly to the D820X.

3.3 DIL-Switch Functions

- Switch 1: RECORD ENABLE
  Defines the polarity of RECEN (see section 3.4)
  OFF : RECORD enabled when
  - low level at RECEN pin
  ON : RECORD enabled when
  - high level at RECEN pin or input open

- Switch 2: AUDIO MUTE
  OFF : MUTE Commands are enabled
  ON : no MUTE commands are sent to the D820X

All other switches should be in OFF position.

Default Settings: all switches in OFF position.

3.4 Additional Features at Slave Control B Connector

RECEN (Pin2):
This signal is used to enable/disable the RECORD function with an external hardware. According to DIL-Switch position 1 and the level of the signal RECEN, RECORD commands are passed to the slave or modified to PLAY.

BURSPD (Pin4), VSRSPD (Pin5), REFIN (Pin13):
An external varispeed control can be connected to the above signals. As long as no synchronizer function is selected, they are looped to the D820X synchronizer connector.

REL1 (Pin6), REL2 (Pin7):
A general purpose relay is controlled by EVON/EVOFF commands. The switch REL1/REL2 is closed with the command EVON.

FAD1 (Pin9), FAD2 (Pin10):
The FADER START lines are connected to the D820's input during synchronizer OFF mode.

MVCL (Pin21), MVDR (Pin24):
Move information of the D820X is provided for master tally wiring: MVDR: LOW = forward
MVCL: 8Hz @ fs = 48kHz

3.5 LED Diagnostic Display

Two LEDs are situated at the front of the interface board. They provide information about the result of the initial selftest and the online status.

An initialization procedure is executed after reset and the main hardware devices are tested. Any resulting error is signalled with a blinking LED (about 2Hz).

DL 1 2 (# = LED blinking, - = LED off)

DL1	DL2	
#	#	RAM test failed.
#	-	Any I/O chip defect

If no error was found, the LEDs signal the communication status of the links to synchronizer board and slave machine.

DL 1 2 (* = LED on, - = LED off)

DL1	DL2	
*	*	communication with synchronizer board failed
*	-	communication with D820X failed
-	*	D820X: TAPEOUT status
-	-	correct operation status

3.6 Application Hints

Remote switching of the TLS power supply is possible.

The tapeout condition may be detected with a delay up to 15sec.

The D820X is controlled with an external frequency until the difference is less than 200usec. The TLS then switches to the D820X's reference, which has to be also the master's one. The TLS control is reactivated as soon as the difference exceeds tha SYNC WINDOW.
During synchronisation modes, the MUTE OFF commands are delayed until the machine reports an "audio ready" condition (TT-LOCK).

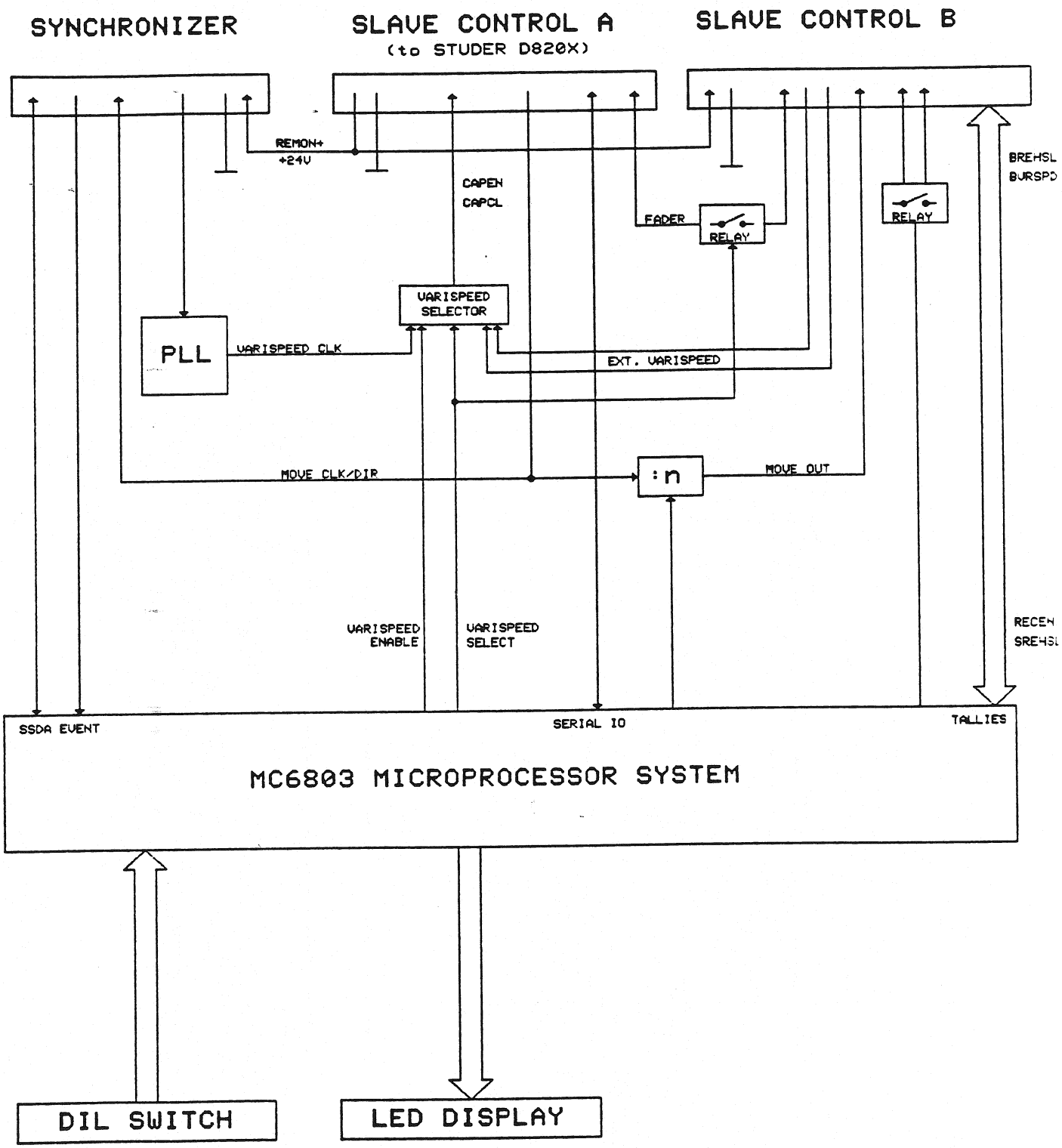
The following recommendations should be considered for operation:
After switching on the D820X, the recorder has to be initialized before changing to a LOCK mode. This may be done by a PLAY command (until timecode is read) and an additional selection of "external sync' mode.

Any modification of the machine's setup or mode should be avoided during synchronizer operation.

The system should only be switched off when in OFF mode.

4 Service Instructions

4.1 Block diagram



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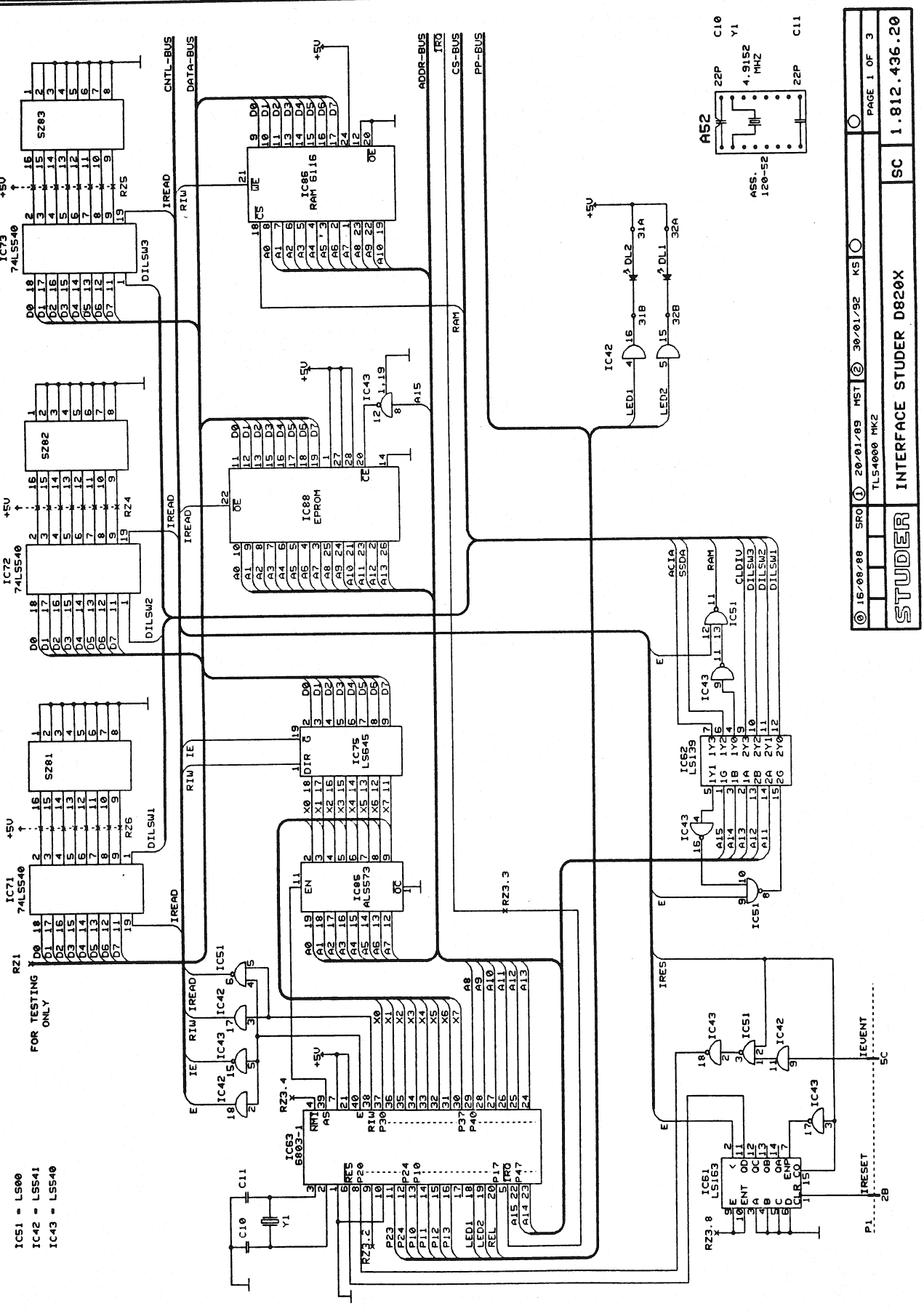
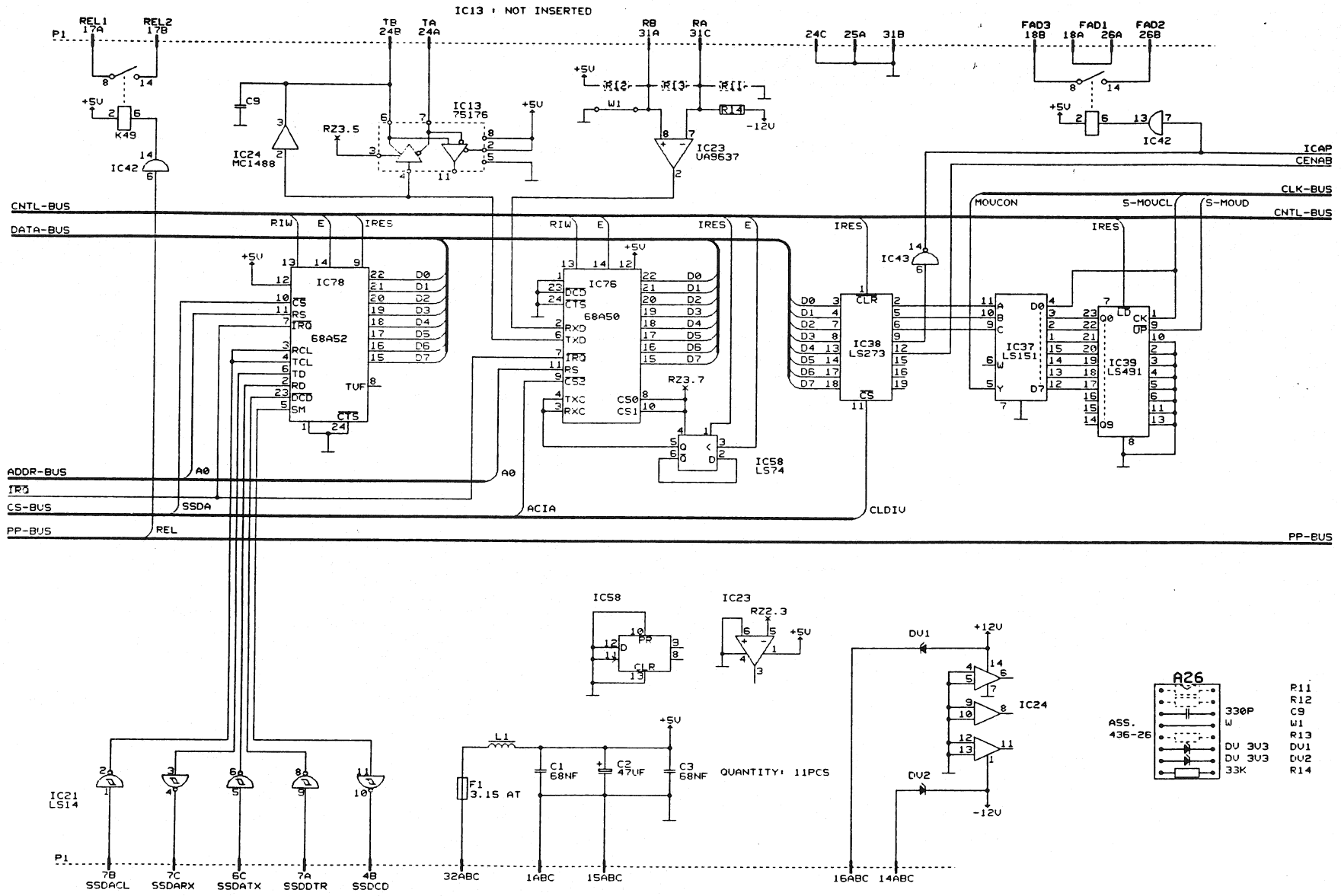
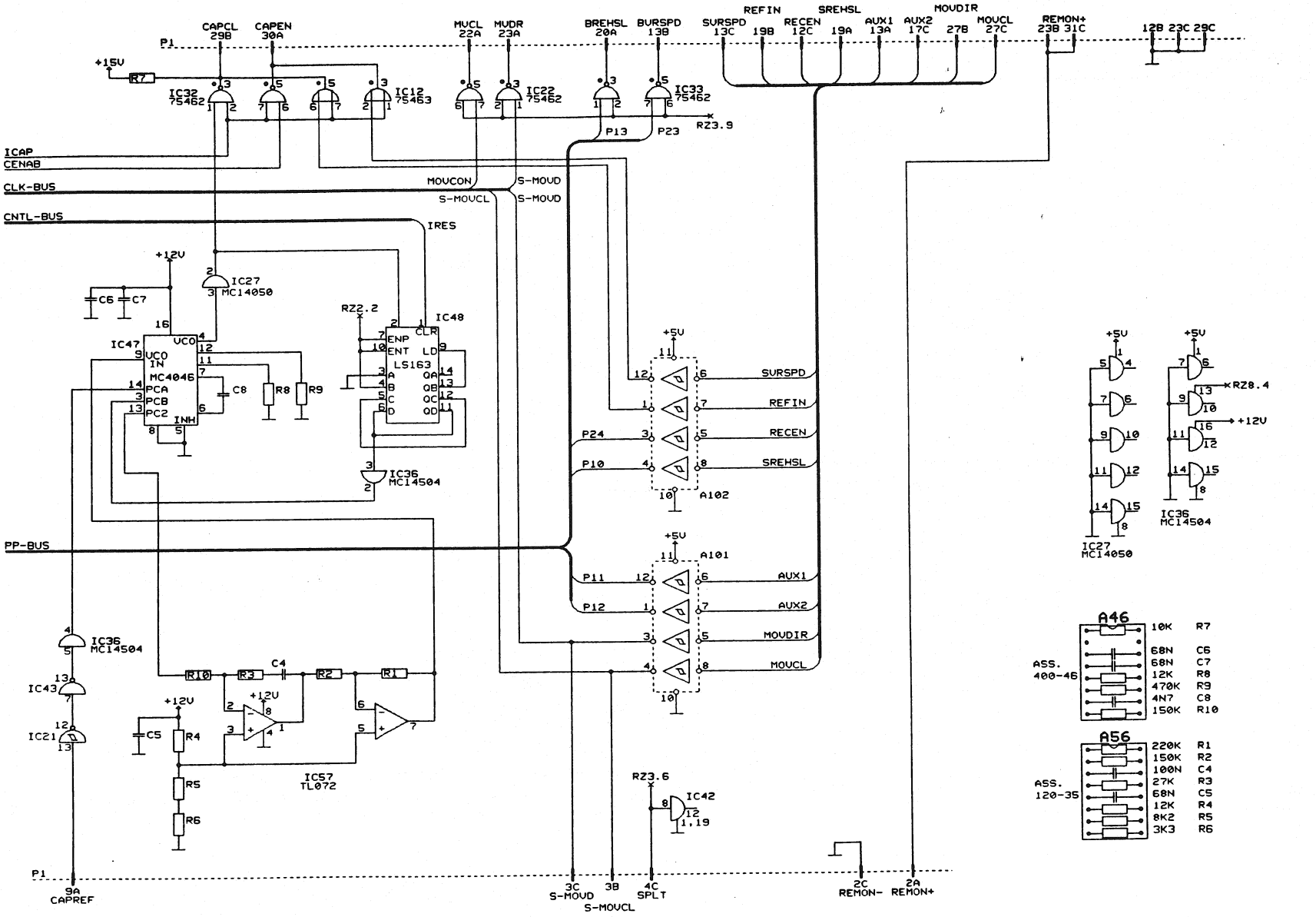
	TLS 4000 MK2			PAGE 1 OF 1
STUDER	INTERFACE STUDER D820X		BL	1.812.436.20

4.2 Diagrams


IC72,IC73,SZ82,SZ83,RZ4,RZ5 = NOT INSERTED
IC1 = LS00
IC42 = LS541
IC43 = LS540
FOR TESTING ONLY
CNTL-BUS
DATA-BUS
ADDR-BUS
CS-BUS
PP-BUS
IRQ
IREAD
RIW
IE
IRES
IEVENT
IRESET
RAM
IC72 74LS540
IC73 74LS540
IC71 74LS540
IC88 EPROM
IC86 RAM 6116
IC75 LS645
IC85 ALS573
IC63 6803-1
IC61 LS163
IC62 LS139
IC51
IC42
IC43
SZ83
SZ82
SZ81
RZ5
RZ4
RZ6
RZ1
DILSW3
DILSW2
DILSW1
A52
4.9152 MHZ
22P
DL2
DL1
LED1
LED2
CLDIV
ACIA SSDA
STUDER
INTERFACE STUDER D820X
TLS4000 MK2
20/01/89 MST
30/01/92 KS
16/08/88 SR0
SC
1.812.436.20
PAGE 1 OF 3

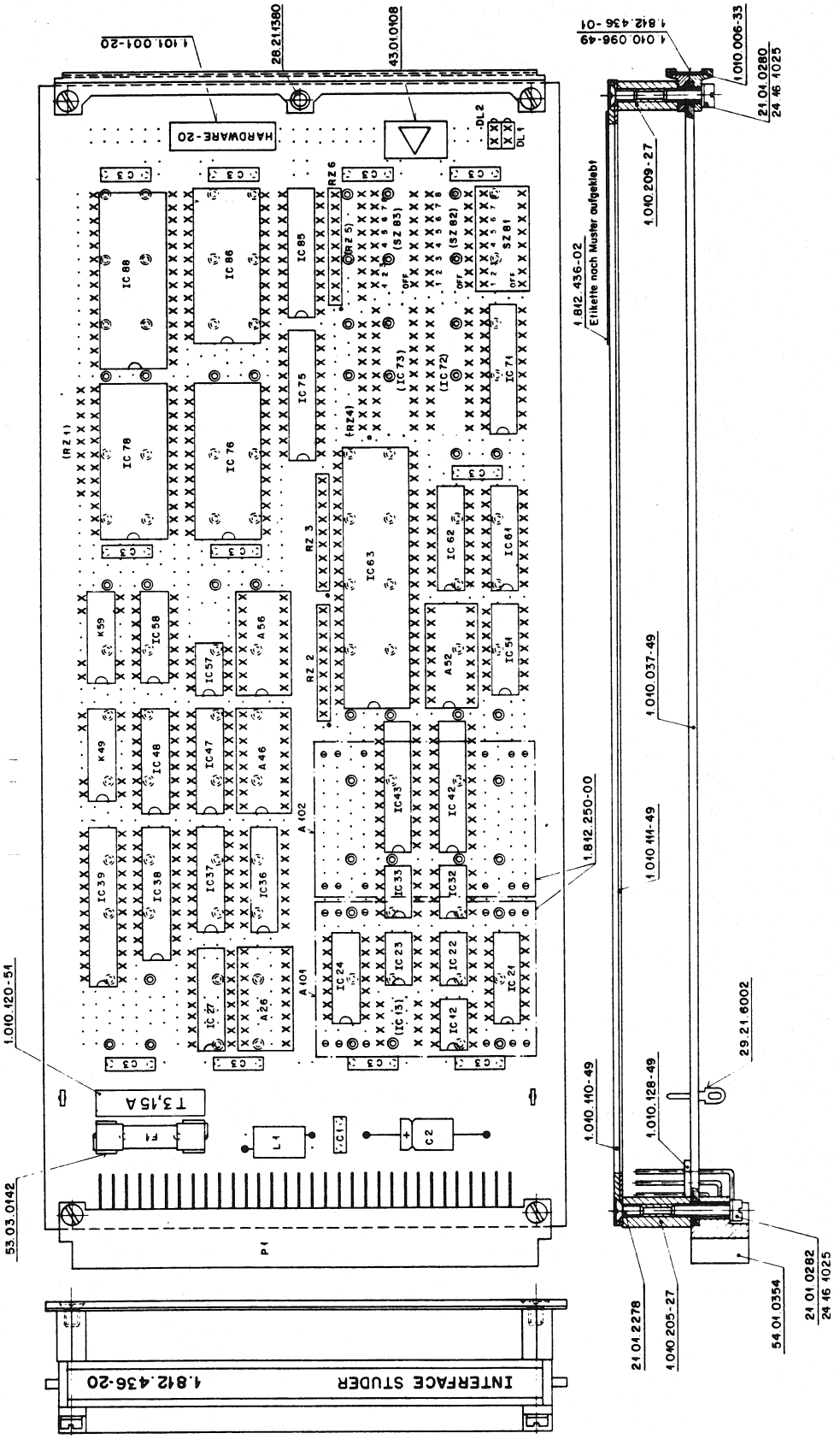


⓪ 16/08/88 SRO	① 20/01/89 MST	② 30/01/92 KS	○		○
	TLS4000 MK2				PAGE 2 OF 3
STUDER	INTERFACE STUDER D820X			SC	1.812.436.20



⓪ 16/08/88 SRO	① 20/01/89 MST	② 30/01/92 KS		
	TLS4000 MK2		PAGE 3 OF 3	
STUDER	INTERFACE STUDER D820X		SC	1.812.436.20

4.3 Component arrangement



4.4 Component position list

IF STUDER D820X 1.812.436.20

Ad	..POS..	...REF.No...		DESCRIPTION.....	MANUFACTURER
	A....26	1.812.231.00		Assembly 436-26	St
	A....46	1.812.213.00		Assembly 400-46	St
	A....52	1.812.201.00		Assembly 120-52	St
	A....56	1.812.203.00		Assembly 120-35	St
	A...101	1.812.250.00		Input Network	St
	A...102	1.812.250.00		Input Network	St
	C.....1	59.99.0205	68 nF	-20%, 63V , CER	
	C.....2	59.25.3470	47 uF	-20%, 16V , EL	
	C.....3	59.99.1200	68 nF	20%, 63V , PET Quantity: 11	
	DL....1	50.04.2107		LED red ,555-2007	Di
	DL....2	50.04.2107		LED red ,555-2007	Di
	F.....1	51.01.0122	3.15 AT	250V, 5 * 20	
	IC...12	50.05.0203		SN 75 463 JG, DS 75 463	
	IC...21	50.06.0014		SN 74 LS 14	
	IC...22	50.05.0227		SN 75 462 JG, SN 75 472 P	
	IC...23	50.15.0114		uA 9637 ACP ,A	
	IC...24	50.15.0106		MC 1488 P, DS 1488	
	IC...27	50.07.0050		MC 14050	
	IC...32	50.05.0227		SN 75 462 JG, SN 75 472 P	
	IC...33	50.05.0227		SN 75 462 JG, SN 75 472 P	
	IC...36	50.15.0103		MC 14504	
	IC...37	50.06.0151		SN 74 LS 151	
	IC...38	50.06.0273		SN 74 LS 273	
	IC...39	50.06.0491		SN 74 LS 491	
	IC...42	50.06.0541		SN 74 LS 541	
	IC...43	50.06.0540		SN 74 LS 540	
	IC...47	50.07.0046		CD 4046 BE, MC 14046 BCP ,A	RCA,Mot
	IC...48	50.06.0163		SN 74 LS 163	
	IC...51	50.06.0000		SN 74 LS 00	
	IC...57	50.09.0101		TL 072 CP	TI
	IC...58	50.06.0074		SN 74 LS 74	
	IC...61	50.06.0163		SN 74 LS 163	
	IC...62	50.06.0139		SN 74 LS 139	
	IC...63	50.16.0107		MC 6803P-1, HD 6803P-1 ,A	Mot,Hi
	IC...71	50.06.0540		SN 74 LS 540	
	IC...75	50.06.0645		SN 74 LS 645	
	IC...76	50.16.0101		MC 68A50 P ,A	
	IC...78	50.16.0114		MC 68A52 P ,A	
	IC...85	50.06.1573		SN 74ALS 573	
	IC...86	50.14.0107		HM 6116 LP-4, SRAM 2k x 8, 200nsec	
	IC...88	50.14.0125	see note	HM 4827128 G-25, EPROM 16k x 8, 300nsec	
	K....49	56.02.1003	5 V 1*A	100V/0.5A, Print	
	K....59	56.02.1003	5 V 1*A	100V/0.5A, Print	
	L.....1	62.01.0115		Wide Band HF-Choke	
	P.....1	54.01.0354		Card Connector 3 * 32 Euro Wrap	
	RZ....2	57.88.4332	8 * 3.3K	2%, Single Line	
	RZ....3	57.88.4332	8 * 3.3K	2%, Single Line	
	RZ....6	57.88.4332	8 * 3.3K	2%, Single Line	
	SZ...81	55.01.0168		8 * ON, DIL-Switch	

Notes : Software release 1.812.969.20 (IC 88)

The following elements are not inserted :
IC 13,72,73
RZ 4,5
SZ 82,83

CER = Ceramic, EL = Electrolytic, PET = Mat. Polyester

MANUFACTURERS : Di = Dialco
Hi = Hitachi
Mot = Motorola
RCA = RCA Corporation
St = Studer
TI = Texas Instruments

1.812.436.20 INTERFACE STUDER D820X KS 88/08/1600

4.5 Signal Description Slave Connectors

SLAVE CONTROL A:

Pin	Signal	Type	Description
1	GND		0.0V
2	TA		n.c.
3	TB	RS232 out	serial data line to D820X
4	GND		0.0V
5	GND		0.0V
6	-		
7	-		
8	FAD1	curr. loop	FADER START command
9	FAD2	curr. loop	FADER START command
10	-		
11	-		
12	MOVDIR	a.l. in	move direction from D820X
13	MOVCL	a.l. in	move clock from D820X
14	-		
15	-		
16	-		
17	-		
18	CAPCL	o.c. out	capstan clock
19	GND		0.0V
20	CAPEN	o.c. out	capstan varispeed enable
21	-		
22	RA	RS232 in	serial data line from D820X
23	RB		n.c.
24	GND		0.0V
25	REMON+		supply voltage from D820X (24V)

o.c. out open collector output, max 28V/0.3A
(no internal pullup resistor)

a.l. in activ low input, driven by open collector or TTL output, or by a switch to GND.
(activ: < 1V, inactiv > 2V or open)
U max: +80V / U min: -20V

curr. loop current loop FAD1-FAD3, max 24V AC/DC

SLAVE CONTROL B: (see section 3.4)

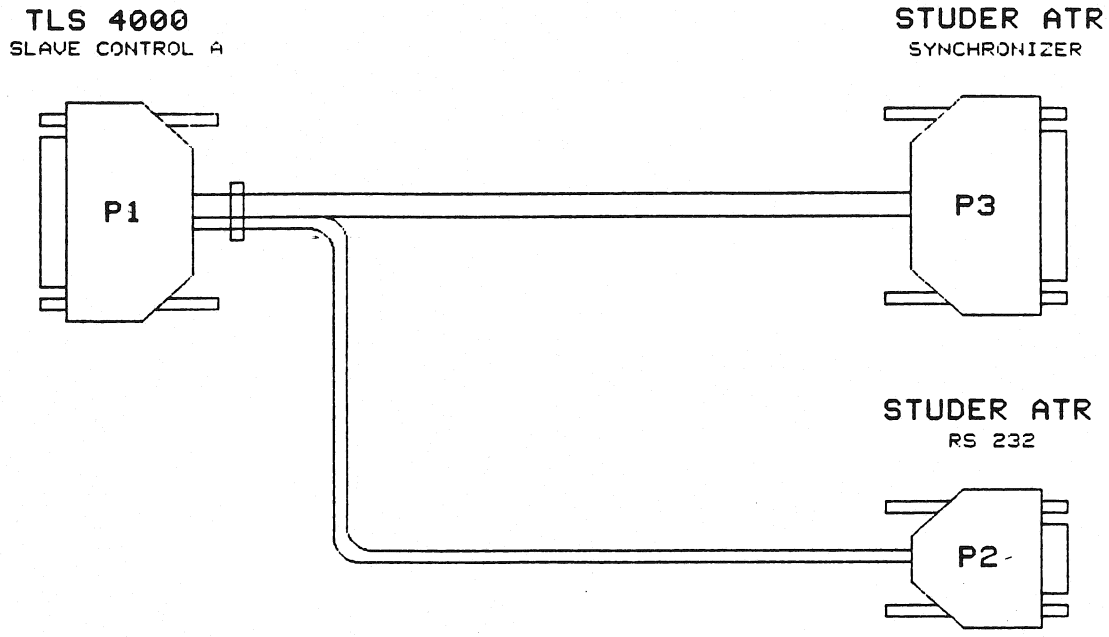
Pin	Signal	Type	Description
1	GND		0.0V
2	RECEN	a.l. in	record enable (see DIL switch 1)
3	AUX1	a.l. in	n.c.
4	BVRSPD	o.c. out	varispeed enabled
5	VSRSPD	a.l. in	external varispeed command
6	REL1		event relay contact 100V/0.5A
7	REL2		event relay contact 100V/0.5A
8	AUX2	a.l. in	n.c.
9	FAD1	curr. loop	FADER START command
10	FAD3	curr. loop	FADER START command (switched)
11	-		
12	SREHSL	a.l. in	rehearsal command
13	REFIN	a.l. in	external varispeed frequency
14	-		
15	BREHSL	o.c. out	rehearsal mode tally
16	-		
17	-		
18	-		
19	-		
20	-		
21	MVCL	o.c. out	move clock
22	-		
23	-		
24	MVDR	o.c. out	move direction
25	VCC		supply voltage D820X (24V)

o.c. out open collector output, max 28V/0.3A
(no internal pullup resistor)

a.l. in activ low input, driven by open collector or TTL output, or by a switch to GND.
(activ: < 1V, inactiv > 2V or open)
U max: +80V / U min: -20V

curr. loop current loop FAD1-FAD3, max 24V AC/DC

4.6 Interface cable for STUDER D820x



P1. 1	GND	P3. 1
8	FAD1	11
9	FAD2	12
12	MOVDIR	10
13	MOVCL	7
18	CAPCL	13
20	CAPEN	5
25	REMON+	25
19	SCREEN	

2	TA	P2. 3
3	TB (RX)	8
5	GND (GND)	9
22	RA (TX)	2
23	RB	7
4	SCREEN	

⓪ 23/01/90 PG			
	TLS 4000 MKII		PAGE 1 OF 1
STUDER	IF-CABLE STUDER D-820X	Z	1.023.758.00